PATENT
Attorney Docket No. 401558/SAKAI

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

TAKAO HASEGAWA

Application No. Unassigned

Art Unit: Unassigned

Examiner: Unassigned

Filed: February 13, 2002

For: METHOD OF WIRING SEMICONDUCTOR INTEGRATED CIRCUIT, SEMICONDUCTOR INTEGRATED CIRCUIT, AND COMPUTER PRODUCT

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Prior to the examination of the above-identified patent application, please enter the following amendments and consider the following remarks.

IN THE SPECIFICATION:

Replace the paragraph beginning at page 2, line 19 with:

An insulation layer is disposed between the first layer and the second layer, thereby to insulate the wirings belonging to one layer from those of the other layer. It is necessary to electrically connect between the a-wiring 1 and the A-wiring 8, and between the a-wiring 2 and the A-wiring 8 respectively, as these wirings handle the same signal. For this purpose, the a-wiring 1 and the A-wiring 8 are connected to each other via the through-hole 5, and the a-wiring 2 and the A-wiring 8 are connected to each other via the through-hole 6. These through-holes are provided to pierce through the insulation layer sandwiched between the first layer and the second layer, in a direction perpendicular to the circuit surface, respectively. Therefore, it is possible to secure electric conduction between the first layer and the second layer through these through-holes. In order to provide these through-holes, according to a conventional automatic wiring, wiring patterns are set subject to a condition that one through-hole is disposed without exception to a pair of these wirings to be connected to each other. Specifically, in the automatic wiring, a setting area is provided on one of the

pair of wirings that needs to be electrically connected to each other, and a corresponding area as a projection of the setting area is provided on the other wiring. With this arrangement, a through-hole is set in a shape that pierces through the insulation layer, and the setting area and the corresponding areas are connected to each other.

Replace the paragraph beginning at page 3, line 21 with:

However, along with the request for making devices smaller in recent years, there has been progress in reduction in the size of a circuit element and a reduction in the width of wiring. As shown in Fig. 11, a through-hole is set to have a smaller width than that of wiring. Therefore, a cross-sectional area of one through-hole per circuit surface also becomes smaller, corresponding to the reduction in the wiring width. Further, according to the conventional automatic wiring, only one through-hole for electric conduction is provided for a pair of wirings that are disposed in different layers.

Replace the paragraph beginning at page 4, line 6 with:

The electric resistance of a through-hole is inversely proportional to cross-sectional area of the through-hole. Therefore, as the reduction in size of a semiconductor integrated circuit has progressed, the resistance of the through-hole has increased, and a current flow has become more difficult.

Replace the paragraph beginning at page 4, line 24 with:

Further, in general, it has been known that electromigration resistance is lowered in inverse proportion to the square of current density. The current density of a through-hole having a smaller cross-section increases when the same level of current flows. This brings about a problem in that the electromigration resistance is lowered.

IN THE CLAIMS:

Replace the indicated claims with:

1. (Amended) A method of wiring a semiconductor integrated circuit having a first layer and a second layer, the method comprising:

disposing a first wiring on a first layer of a semiconductor integrated circuit and disposing a second wiring on a second layer of said semiconductor integrated circuit, wherein said first and second wirings are arranged subject to a condition that a predetermined number

of through-holes are to extend between said first and second wirings, connecting said first and second layers to each other;

searching for a setting area in one of said first and second layers, and a corresponding area in the other of said first and second layers as a projection of the setting area, that enable setting of an additional through-hole between said first and second wiring; and

setting the additional through-hole between the setting area and the corresponding area.

2. (Amended) The method of wiring a semiconductor integrated circuit according to claim 1, wherein, in setting the additional through-hole, giving the additional through-hole the same shape as the predetermined number of through-holes.

3. (Amended) The method of wiring a semiconductor integrated circuit according to claim 1, wherein, in setting the additional through-hole, choosing shape of the additional through-hole based on shape of the setting area.

4. (Amended) A method of wiring a semiconductor integrated circuit having a first layer and a second layer, the method comprising:

disposing a first wiring on a first layer of a semiconductor integrated circuit and disposing a second wiring on a second layer of said semiconductor integrated circuit, wherein said first and second wirings are arranged subject to a condition that a predetermined number of through-holes are to extend between said first and second wirings, connecting said first and second layers to each other;

searching for a setting area in said first layer, and a corresponding area in said second layer as a projection area of the setting area, that enable setting of an additional through-hole between said first and second wiring;

disposing an additional wiring for setting the additional through-hole in either the setting area or the corresponding area; and

setting the additional through-hole to extend between the setting area and the corresponding area.

5. (Amended) The method of wiring a semiconductor integrated circuit according to claim 4, wherein,

in searching for a setting area, searching under a condition that the setting area is a part of the area in which said first wiring has been disposed, and that the corresponding area is an area that is close to said second wiring and an area in which no wiring or circuit element exists, and

in arranging the additional wiring, extending said second wiring to the corresponding area.

6. (Amended) The method of wiring a semiconductor integrated circuit according to claim 4, wherein,

in searching for a setting area, searching under a condition that the setting area is an area that is close to said first wiring on said first layer and in which no wiring or circuit element exists, and the corresponding area is an area that is close to said second wiring on said second layer and in which no wiring or circuit element exists, and

in disposing the additional wiring, extending said first wiring on said first layer to the setting area, and extending said second wiring on said second layer to the corresponding area.

7. (Amended) The method of wiring a semiconductor integrated circuit according to claim 4, wherein, in setting the additional through-hole, making the shape of the additional through-hole the same as the shape of through-hole.

8. (Amended) The method of wiring a semiconductor integrated circuit according to claim 4, wherein, in setting the through-hole, choosing a shape of the additional through-hole based on shape of the setting area.

9. (Amended) A semiconductor integrated circuit comprising:

a multi-layer structure including a first layer and a second layer;

a setting area disposed on said first layer;

a corresponding layer disposed on said second layer as a projection of said setting area; and

a through-hole which connects said setting area and said corresponding area, said through-hole having a shape corresponding to shapes of said setting area and said corresponding area.

10. (Amended) A computer program containing instructions which, when executed on a computer causes the computer to design wiring of a semiconductor integrated circuit, having a first layer and a second layer, the method comprising:

disposing a first wiring on a first layer of a semiconductor integrated circuit and disposing a second wiring on a second layer of said semiconductor integrated circuit, wherein said first and second wirings are arranged subject to a condition that a predetermined number of through-holes are to extend between said first and second wirings, connecting said first and second layers to each other;

searching for a setting area in one of said first and second layers, and a corresponding area in the other of said first and second layers as a projection of the setting area, that enable setting of an additional through-hole between said first and second wiring; and

setting the additional through-hole between the setting area and the corresponding area.

11. (Amended) A computer program containing instructions which when executed on a computer, causes the computer to design wiring of a semiconductor integrated circuit, having a first layer and a second layer, the method comprising:

disposing a first wiring on a first layer of a semiconductor integrated circuit and disposing a second wiring on a second layer of said semiconductor integrated circuit, wherein said first and second wirings are arranged subject to a condition that a predetermined number of through-holes are to extend between said first and second wirings, connecting said first and second layers to each other;

searching for a setting area in said first layer, and a corresponding area in said second layer as a projection area of the setting area, that enable setting of an additional through-hole between said first and second wiring;

disposing an additional wiring for setting the additional through-hole in either the setting area or the corresponding area; and

setting the additional through-hole to extend between the setting area and the corresponding area.

IN THE ABSTRACT:

Replace the Abstract with:

<u>ABSTRACT OF THE DISCLOSURE</u>

The wiring method includes determining wirings based on a condition that one through-hole is formed; picking up a pair of wirings that are disposed on different layers and that need to be electrically connected to each other, from among the determined wirings, and extracting areas occupied by the wirings; making a decision about whether there exist areas that coincide with each other between the wirings; making a decision about whether the coincident areas have space sufficient for an additional through-hole; and setting an additional through-hole on the coincident areas with sufficient space.

REMARKS

The foregoing Amendment corrects translational errors and conforms the claims to United States practice. No new matter is added.

Respectfully submitted,

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Art Unit: Unassigned

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AMENDMENTS TO SPECIFICATION, CLAIMS AND ABSTRACT MADE VIA PRELIMINARY AMENDMENT

Amendments to the paragraph beginning at page 2, line 19:

An insulation layer is disposed between the first layer and the second layer, thereby to insulate the wirings belonging to one layer from those of the other layer. It is necessary to electrically connect between the a-wiring 1 and the A-wiring 8, and between the a-wiring 2 and the A-wiring 8 respectively, as these wirings handle the same signal. For this purpose, the a-wiring 1 and the A-wiring 8 are connected to each other via the through-hole 5, and the a-wiring 2 and the A-wiring 8 are connected to each other via the through-hole 6. These through-holes are provided to pierce through the insulation layer sandwiched between the first layer and the second layer, in a direction perpendicular to the circuit surface, respectively. Therefore, it is possible to secure ~~an~~ electric conduction between the first layer and the second layer through these through-holes. In order to provide these through-holes, according to a conventional automatic wiring, wiring patterns are set subject to a condition that one through-hole is disposed without exception to a pair of these wirings to be connected to each other. Specifically, in the automatic wiring, a setting area is provided on one of the pair of wirings that ~~need~~ needs to be electrically connected to each other, and ~~an~~ a corresponding area as a projection of the setting area is provided on the other wiring. With this arrangement, a through-hole is set in a shape that pierces through the insulation layer, and the setting area and the corresponding ~~area~~ areas are connected to each other.

Amendments to the paragraph beginning at page 3, line 21:

However, along with the request for ~~fining a device~~ making devices smaller in recent years, there ~~have~~ has been ~~progressed a~~ progress in reduction in the size of a circuit element and a reduction in the width of wiring. As shown in Fig. 11, a through-hole is set to have a smaller width than that of wiring. Therefore, a cross-sectional area of one through-hole per circuit surface also becomes ~~small~~ smaller, corresponding to the reduction in the wiring width. Further, according to the conventional automatic wiring, only one through-hole for electric conduction is provided ~~to~~ for a pair of wirings that are disposed ~~on~~ in different layers.

Amendments to the paragraph beginning at page 4, line 6:

~~In the mean time,~~The electric resistance of a through-hole is inversely proportional to ~~a~~ cross-sectional area of the through-hole. Therefore, ~~when~~ as the ~~fining~~ reduction in size of a semiconductor integrated circuit ~~is~~ has progressed, the resistance of the through-hole ~~increases~~ has increased, and a current ~~becomes~~ flow has become more difficult ~~to flow~~.

Amendments to the paragraph beginning at page 4, line 24:

Further, in general, it has been known that electromigration ~~proof~~ resistance is lowered in ~~inversely proportional~~ inverse proportion to the square of current density. The current density of a through-hole having a smaller cross-section increases when the same level of current flows. This brings about a problem in that the electromigration ~~proof~~ resistance is lowered.

Amendments to existing claims:

1. (Amended) A method of wiring a semiconductor integrated circuit~~, said semiconductor integrated circuit~~ having a first layer and a second layer, the method comprising ~~the steps of~~:

disposing a first wiring on ~~said~~ a first layer of a semiconductor integrated circuit and disposing a second wiring on ~~said~~ a second layer of said semiconductor integrated circuit, wherein said first and second wirings are ~~disposed~~ arranged subject to a condition that a predetermined number of through-holes are ~~set~~ to extend between said first and second wirings, ~~and~~ connecting said first and second layers ~~being electrically connected~~ to each other;

searching for a setting area in one of said first and second layers, and ~~an~~ a corresponding area in the other of said first and second layers as a projection ~~area~~ of the

setting area, that enable ~~a~~ setting of ~~new other~~ an additional through-hole between said first and second wiring ~~that have been determined~~; and

setting the ~~new other~~ additional through-hole between ~~said~~ the setting area and ~~said~~ the corresponding area.

2. (Amended) The method of wiring a semiconductor integrated circuit according to claim 1, wherein ~~at~~, in setting the additional through-hole ~~setting step, the shape of said new other~~ giving the additional through-hole ~~is the same as~~ the same shape ~~of said through-hole that has been set at the wiring step~~ as the predetermined number of through-holes.

3. (Amended) The method of wiring a semiconductor integrated circuit according to claim 1, wherein ~~at~~, in setting the additional through-hole ~~setting step, the~~ choosing shape of ~~said new other~~ the additional through-hole ~~is decided~~ based on ~~a~~ shape of ~~said~~ the setting area.

4. (Amended) A method of wiring a semiconductor integrated circuit~~, said semiconductor integrated circuit~~ having a first layer and a second layer, the method comprising:

~~a first wiring step of~~ disposing a first wiring on ~~said~~ a first layer of a semiconductor integrated circuit and disposing a second wiring on ~~said~~ a second layer of said semiconductor integrated circuit, wherein said first and second wirings are ~~disposed~~ arranged subject to a condition that a predetermined number of through-holes are ~~set~~ to extend between said first and second wirings, ~~and~~ connecting said first and second layers ~~being electrically connected~~ to each other;

~~an area searching step of~~ searching for a setting area in said first layer, and ~~an~~ a corresponding area in said second layer as a projection area of the setting area, that enable ~~a~~ setting of ~~new other~~ an additional through-hole between said first and second wiring ~~that have been determined~~;

~~a second wiring step of~~ disposing an additional wiring for setting the ~~other~~ additional through-hole in either ~~said searched~~ the setting area or ~~said searched~~ the corresponding area; and

~~a through-hole setting step of~~ setting the ~~new other~~ additional through-hole to extend between ~~said~~ the setting area and ~~said~~ the corresponding area.

5. (Amended) The method of wiring a semiconductor integrated circuit according to claim 4, wherein,

~~at the area~~ in searching ~~step~~ for a setting area, ~~the search is made~~ searching under a condition that ~~said~~ the setting area ~~that is searched for~~ is a part of the area in which said first

wiring has been disposed, and that ~~said~~ the corresponding area ~~that is searched for~~ is an area that is close to said second wiring and ~~the~~ an area in which no wiring or circuit element exists, and

~~at the second wiring step~~ in arranging the additional wiring, extending said second wiring ~~is extended~~ to ~~said~~ the corresponding area.

6. (Amended) The method of wiring a semiconductor integrated circuit according to claim 4, wherein,

~~at the area~~ in searching ~~step~~ for a setting area, ~~the search is made~~ searching under a condition that ~~said~~ the setting area ~~that is searched for~~ is an area that is close to said first wiring on said first layer, and ~~the area~~ in which no wiring or circuit element exists, and ~~that said~~ the corresponding area ~~that is searched for~~ is an area that is close to said second wiring on said second layer, and ~~the area~~ in which no wiring or circuit element exists, and

~~at the second wiring step~~ in disposing the additional wiring, extending said first wiring on said first layer ~~is extended~~ to ~~said~~ the setting area, and extending said second wiring on said second layer ~~is extended~~ to ~~said~~ the corresponding area.

7. (Amended) The method of wiring a semiconductor integrated circuit according to claim 4, wherein ~~at the through-hole~~, in setting ~~step~~ the additional through-hole, making the shape of ~~said new other~~ the additional through-hole ~~is~~ the same as the shape of ~~said~~ through-hole ~~that has been set at the first wiring step~~.

8. (Amended) The method of wiring a semiconductor integrated circuit according to claim 4, wherein ~~at~~, in setting the through-hole ~~setting step~~, ~~the~~ choosing a shape of ~~said new other~~ the additional through-hole ~~is decided~~ based on ~~a~~ shape of ~~said~~ the setting area.

9. (Amended) A semiconductor integrated circuit comprising:

a multi-layer structure including a first layer and a second layer;

a setting area disposed on said first layer;

a corresponding layer disposed on said second layer as a projection ~~area~~ of said setting area; and

a through-hole which connects ~~between~~ said setting area and said corresponding area, said through-hole having a shape corresponding to ~~the~~ shapes of said setting area and said corresponding area.

10. (Amended) A computer program containing instructions which, when executed on a computer causes the computer to ~~realize a method of~~ design wiring of a semiconductor

integrated circuit, ~~said semiconductor integrated circuit~~ having a first layer and a second layer, the method comprising ~~the steps of~~:

disposing a first wiring on ~~said~~ a first layer of a semiconductor integrated circuit and disposing a second wiring on ~~said~~ a second layer of said semiconductor integrated circuit, wherein said first and second wirings are ~~disposed~~ arranged subject to a condition that a predetermined number of through-holes are ~~set~~ to extend between said first and second wirings, ~~and~~ connecting said first and second layers ~~being electrically connected~~ to each other;

searching for a setting area in one of said first and second layers, and ~~an~~ a corresponding area in the other of said first and second layers as a projection ~~area~~ of the setting area, that enable ~~a~~ setting of ~~new other~~ an additional through-hole between said first and second wiring ~~that have been determined~~; and

setting the ~~new other~~ additional through-hole between ~~said~~ the setting area and ~~said~~ the corresponding area.

11. (Amended) A computer program containing instructions which when executed on a computer, causes the computer to ~~realize a method of~~ design wiring of a semiconductor integrated circuit, ~~said semiconductor integrated circuit~~ having a first layer and a second layer, the method comprising ~~the steps of~~:

~~a first wiring step of~~ disposing a first wiring on ~~said~~ a first layer of a semiconductor integrated circuit and disposing a second wiring on ~~said~~ a second layer of said semiconductor integrated circuit, wherein said first and second wirings are ~~disposed~~ arranged subject to a condition that a predetermined number of through-holes are ~~set~~ to extend between said first and second wirings, ~~and~~ connecting said first and second layers ~~being electrically connected~~ to each other;

~~an area searching step of~~ searching for a setting area in said first layer, and ~~an~~ a corresponding area in said second layer as a projection area of the setting area, that enable ~~a~~ setting of ~~new other~~ an additional through-hole between said first and second wiring ~~that have been determined~~;

~~a second wiring step of~~ disposing an additional wiring for setting the ~~other~~ additional through-hole in either ~~said searched~~ the setting area or ~~said searched~~ the corresponding area; and

~~a through-hole setting step of~~ setting the ~~new other~~ additional through-hole to extend between ~~said~~ the setting area and ~~said~~ the corresponding area.

Amendments to the abstract:

ABSTRACT OF THE DISCLOSURE

The wiring method includes determining wirings based on a condition that one through-hole is formed; picking up a pair of wirings that are disposed on different layers and that need to be electrically connected to each other, from among the determined wirings, and extracting areas occupied by the wirings; making a decision about whether ~~or not~~ there exist areas that coincide with each other between the wirings; making a decision about whether ~~or not~~ the coincident areas have space sufficient ~~enough~~ for ~~setting a~~ an additional through-hole; and setting ~~new other~~ an additional through-hole on the coincident areas with sufficient space.

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Art Unit: Unassigned

Examiner: Unassigned

PENDING CLAIMS AFTER ENTRY OF PRELIMINARY AMENDMENT

1. A method of wiring a semiconductor integrated circuit having a first layer and a second layer, the method comprising:

disposing a first wiring on a first layer of a semiconductor integrated circuit and disposing a second wiring on a second layer of said semiconductor integrated circuit, wherein said first and second wirings are arranged subject to a condition that a predetermined number of through-holes are to extend between said first and second wirings, connecting said first and second layers to each other;

searching for a setting area in one of said first and second layers, and a corresponding area in the other of said first and second layers as a projection of the setting area, that enable setting of an additional through-hole between said first and second wiring; and

setting the additional through-hole between the setting area and the corresponding area.

2. The method of wiring a semiconductor integrated circuit according to claim 1, wherein, in setting the additional through-hole, giving the additional through-hole the same shape as the predetermined number of through-holes.

3. The method of wiring a semiconductor integrated circuit according to claim 1, wherein, in setting the additional through-hole, choosing shape of the additional through-hole based on shape of the setting area.

4. A method of wiring a semiconductor integrated circuit having a first layer and a second layer, the method comprising:

disposing a first wiring on a first layer of a semiconductor integrated circuit and disposing a second wiring on a second layer of said semiconductor integrated circuit, wherein said first and second wirings are arranged subject to a condition that a predetermined number of through-holes are to extend between said first and second wirings, connecting said first and second layers to each other;

searching for a setting area in said first layer, and a corresponding area in said second layer as a projection area of the setting area, that enable setting of an additional through-hole between said first and second wiring;

disposing an additional wiring for setting the additional through-hole in either the setting area or the corresponding area; and

setting the additional through-hole to extend between the setting area and the corresponding area.

5. The method of wiring a semiconductor integrated circuit according to claim 4, wherein,

in searching for a setting area, searching under a condition that the setting area is a part of the area in which said first wiring has been disposed, and that the corresponding area is an area that is close to said second wiring and an area in which no wiring or circuit element exists, and

in arranging the additional wiring, extending said second wiring to the corresponding area.

6. The method of wiring a semiconductor integrated circuit according to claim 4, wherein,

in searching for a setting area, searching under a condition that the setting area is an area that is close to said first wiring on said first layer and in which no wiring or circuit element exists, and the corresponding area is an area that is close to said second wiring on said second layer and in which no wiring or circuit element exists, and

in disposing the additional wiring, extending said first wiring on said first layer to the setting area, and extending said second wiring on said second layer to the corresponding area.

7. The method of wiring a semiconductor integrated circuit according to claim 4, wherein, in setting the additional through-hole, making the shape of the additional through-hole the same as the shape of through-hole.

8. The method of wiring a semiconductor integrated circuit according to claim 4, wherein, in setting the through-hole, choosing a shape of the additional through-hole based on shape of the setting area.

9. A semiconductor integrated circuit comprising:

a multi-layer structure including a first layer and a second layer;

a setting area disposed on said first layer;

a corresponding layer disposed on said second layer as a projection of said setting area; and

a through-hole which connects said setting area and said corresponding area, said through-hole having a shape corresponding to shapes of said setting area and said corresponding area.

10. A computer program containing instructions which, when executed on a computer causes the computer to design wiring of a semiconductor integrated circuit, having a first layer and a second layer, the method comprising:

disposing a first wiring on a first layer of a semiconductor integrated circuit and disposing a second wiring on a second layer of said semiconductor integrated circuit, wherein said first and second wirings are arranged subject to a condition that a predetermined number of through-holes are to extend between said first and second wirings, connecting said first and second layers to each other;

searching for a setting area in one of said first and second layers, and a corresponding area in the other of said first and second layers as a projection of the setting area, that enable setting of an additional through-hole between said first and second wiring; and

setting the additional through-hole between the setting area and the corresponding area.

11. A computer program containing instructions which when executed on a computer, causes the computer to design wiring of a semiconductor integrated circuit, having a first layer and a second layer, the method comprising:

disposing a first wiring on a first layer of a semiconductor integrated circuit and disposing a second wiring on a second layer of said semiconductor integrated circuit, wherein said first and second wirings are arranged subject to a condition that a predetermined number of through-holes are to extend between said first and second wirings, connecting said first and second layers to each other;

searching for a setting area in said first layer, and a corresponding area in said second layer as a projection area of the setting area, that enable setting of an additional through-hole between said first and second wiring;

disposing an additional wiring for setting the additional through-hole in either the setting area or the corresponding area; and

setting the additional through-hole to extend between the setting area and the corresponding area.